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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/502,194	ABRAHAM ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/10/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-41 were examined.

Response to Applicants Arguments

Information Disclosure Statement

2. The applicants have not discussed this issue in the response to the first office action. Therefore objection stands.

Response to Claim Rejections - 35 USC § 102 Rejection

3. The applicants are thanked for responding to this issue. Applicant's arguments filed 8/10/04 have been fully considered but they are not persuasive. The applicant states, summarily, that Schlansker et al. (U.S. Patent 6,408,428) does not teach forming a Cartesian product of the component Pareto sets. The examiner rebuffs this statement in that Schlankser teaches a Pareto filter set (column 85 and 87, lines 5-35 and 6-21, respectively) coupled with the teaching of a Cartesian product (column 43, lines 14-31), which is integral to the MDES. The rejection stands.

Response to Claim Rejections - 35 USC § 103 Rejection

4. The applicants have not discussed this issue in the response to the first office action. Therefore the rejection stands.

Rejections

New Matter

5. The amendment filed 8/10/04 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: *FIGS. 8-9 illustrate computer programs that perform validity filtering or quality filtering (or both) on system designs composed of component designs Dj, . . . ,Do. In FIG. 8, respective common component validity filters Cj, . . . ,Cn prepare component validity sets for respective component designs D1, . . . ,Dn. The component validity sets are then filtered by partial component validity filters defined by partial component validity predicates (Vj:, . . . ,V1a), . . ., (Vn1 , . . . ,Vnz), respectively. As noted previously, for any component design space for which all designs are known to be valid, validity filtering can be omitted and if all system designs are known to be valid, validity filtering can be completely omitted. The resulting partial component validity sets are combined to form component validity sets* S_{11}, . . ., S_{nm}. *In steps* 801_1, . . ., 801_m *Cartesian products of these sets form system design sets* S_1., . . . ,S_a S_1,....S_m *that are combined to form a system validity set S..*

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-12, 14-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Schlansker et al. (U.S. Patent 6,408,428 (1999)).

Schlansker et al. teaches a hierarchical approach of evaluating processors (cache) and provides a method to account for each stage of changes (abstract).

Claim 1: A method of programmatically selecting system designs (column 21, lines 9-11) from a system design space (abstract, line 1-5), the method comprising: specifying system designs as combinations of component designs from respective component design spaces; applying component quality filters to the component design spaces to produce component Pareto sets of designs (column 85 and 87, lines 5-35 and 6-21, respectively); and forming a Cartesian product (column 43, lines 14-16) of the

component Pareto (column 85 and 87, lines 5-35 and 6-21, respectively) sets to obtain a set of system designs.

Claim 2: The method of claim 1, further comprising applying component validity filters (column 13, lines 4-9, 16-19, and 50-55) to respective component design spaces before applying the component quality filters, wherein the component quality sets of designs include only designs satisfying respective component validity filters.

Claim 3: The method of claim 1, further comprising applying a system validity filter to the set of system designs to produce a validity filtered set of system designs (column 8, lines 30-36).

Claim 4: The method of claim 3, further comprising applying a system quality filter to the set of system designs (column 13 lines 4-19).

Claim 5: The method of claim 1, further comprising applying a system quality filter to the set of system designs (column 13 lines 4-19).

Claim 6: A method of programmatically selecting system designs that are specified by combinations of component designs (column 7, lines 5-30), the method comprising: preparing component validity sets for each of the component designs by applying component validity filters to corresponding component design spaces, the component

validity filters defined by corresponding component validity predicates; and forming a set of system designs that is a Cartesian product of the component validity sets (column 43, lines 14-16); applying a system quality filter to the Cartesian product of the component validity sets to produce a Pareto set (column 85 and 87, lines 5-35 and 6-21, respectively).

Claim 7: The method of claim 6, wherein the component designs are specified by component parameters, and the component validity filter for each component is independent of the component parameters of other components (column 10, lines 50-63).

Claim 8: The method of claim 6, further comprising applying a system validity filter to the Cartesian product of the component validity sets (column 43, lines 14-16).

Claim 9: The method of claim 6(column 43, lines 14-16), further comprising applying component evaluation function to the validity sets (column 85 and 87, lines 5-35 and 6-21, respectively).

Claim 10: The method of claim 6, further comprising applying a system evaluation function (column 4, lines 16-27) and the system quality filter to the Cartesian product (column 43, lines 14-16) of the component validity sets after applying a system validity filter.

Claim 11: The method of claim 10, further comprising applying a component evaluation (column 4, lines 16-27) function and a component quality filter to the component validity sets (column 14, lines 1-7).

Claim 12: The method of claim 6, further comprising applying a component evaluation function (column 4, lines 16-27) and a component quality filter (column 14, lines 1-7) to at least one of the component validity sets before forming the set of system designs (column 13, lines 57-66).

Claim 14: A method of selecting system designs that are specified by combinations of component designs (column 17, lines 28-35), the method comprising: preparing component validity sets for each of the component designs by applying component validity filters to corresponding component designs (column 13, 50-66) the component validity filters defined by corresponding component validity predicates (column 15, lines 28-40); preparing component Pareto sets (column 85 and 87, lines 5-35 and 6-21, respectively) by applying corresponding component evaluation functions and component quality filters to the component validity sets; and forming a set of system designs that is a Cartesian product (column 43, lines 14-16) of the component Pareto sets(column 85 and 87, lines 5-35 and 6-21, respectively).

Claim 15: The method of claim 14, further comprising applying a system validity filter to the Cartesian product (column 43, lines 14-16) of the component Pareto sets (column 85 and 87, lines 5-35 and 6-21, respectively).

Claim 16: The method of claim 14, further comprising applying a system evaluation function (column 4, lines 16-27) and a system quality filter to the Cartesian product (column 43, lines 14-16) of the component Pareto sets (column 85 and 87, lines 5-35 and 6-21, respectively).

Claim 17: The method of claim 16, wherein the component evaluation functions and the system evaluation function produce component evaluation metrics (column 4, lines 16-27) and system evaluation metrics (columns 83 and 84 VLIW evaluation; column 84, lines 31-45), respectively, and the system evaluation metrics are obtained from the component evaluation metrics.

Claim 18: A computer readable medium comprising computer executable instructions for performing the method of claim 1 (column 16, line 41).

Claim 19: A computer readable medium comprising computer executable instructions for performing the method of claim 6 (column 16, line 41).

Claim 20: A computer readable medium comprising computer executable instructions (column 4, lines 45-48) for performing the method of claim 14.

Claim 21: A method of programmatically selecting a system design from a set of system designs, comprising (column 3, lines 17-24): defining a system validity predicate (column 15, 27-40) that is a function of two or more terms; defining partial validity predicates by expressing the system validity predicate in a canonical form; applying partial validity filters that are defined by the partial validity predicates (column 3, lines 57-60) to the system designs to obtain partial validity sets; and applying a quality filter to the system designs of the partial validity sets to produce respective partial Pareto sets; and combining the partial Pareto (column 85 and 87, lines 5-35 and 6-21, respectively) sets to form a Pareto set.

Claim 22: The method of claim 21, wherein each of the partial validity predicates is in product form (column 42, line 32).

Claim 23: The method of claim 21, wherein the partial (column 3, lines 57-61) validity predicates are mutually exclusive (column 10, lines 33-34).

Claim 24: A method of programmatically selecting a set of system designs (column 21, lines 9-11), comprising: selecting a system validity filter defined by a system validity predicate, the system validity predicate including one or more partial validity predicates

(column 15, lines 28-40) that define partial validity filters; applying the partial validity filters to the system designs (column 3, lines 57-60); forming partial validity sets that include system designs satisfying respective partial validity filters; applying an evaluation function to the system designs of the partial validity sets (column 3, lines 57-60), the evaluation function producing an evaluation (column 4, lines 16-27) metric for each system design; applying a quality filter to the system designs of the partial validity sets, the quality filter comparing and selecting system designs based on the evaluation metrics and producing respective partial Pareto sets (column 85 and 87, lines 5-35 and 6-21, respectively); and combining the partial Pareto sets(column 85 and 87, lines 5-35 and 6-21, respectively) to form a first quality set (column 13, lines 50-66).

Claim 25. The method of claim 24, further comprising applying the quality filter to the first Pareto set (column 85 and 87, lines 5-35 and 6-21, respectively).

Claim 26: The method of claim 24, wherein each of the partial validity (column 3, lines 41-46) predicates (column 15, lines 28-40) is in product form (column 43, lines 14-16).

Claim 27: The method of claim 26, wherein the system validity (column 3, lines 41-46) predicate (column 15, lines 28-40) is a product (column 43, lines 14-16) of the partial validity predicates.

Claim 28: The method of claim 26, wherein the partial validity (column 3, lines 41-46) sets are combined to form (column 4, liners 16-25) two or more system validity sets.

Claim 29: A computer readable medium (column 92, claim 17) having computer executable instructions for performing the method of claim 24.

Claim 30: A computer readable medium having software for performing the (column 16, line 41) method of claim 25.

Claim 31: A method of programmatically selecting a design for a cache memory, comprising: selecting components for the cache memory; determining component Pareto sets for the components (column 85 and 87, lines 5-35 and 6-21, respectively); preparing a combined Pareto set from the component Pareto sets (column 85 and 87, lines 5-35 and 6-21, respectively); and selecting a cache memory design from the combined Pareto set.

Claim 32: A method of selecting a design for a processor system, the processor system including a processor and a cache memory (column 31, lines 65-66), the method comprising: preparing a component Pareto set for the processor; preparing a component Pareto set (column 85 and 87, lines 5-35 and 6-21, respectively) for a cache memory; preparing a combined Pareto set from the component Pareto sets (column 85 and 87, lines 5-35 and 6-21, respectively) of the processor and the cache memory; and

selecting a processor system design from the combined Pareto set (column 85, lines 16-36).

Claim 33: A method of programmatically generating a set of designs for a processor system, comprising: dividing the processor system into at least a processor component and a memory component; preparing component validity sets for the processor component and the memory component (column 16, lines 39-52); preparing component Pareto sets (column 85 and 87, lines 5-35 and 6-21, respectively) for the processor component and the memory component: and forming a Cartesian product (column 43, lines 14-16) of the component Pareto sets (column 85 and 87, lines 5-35 and 6-21, respectively) to produce the set of designs for the processor system validity set.

Claim 34: The method of claim 33, further comprising applying a system evaluation function and a system quality filter to the Cartesian product of the component Pareto sets (column 85 and 87, lines 5-35 and 6-21, respectively).

Claim 35: A method of designing a processor system that includes a processor component and a memory component (column 31, lines 65-66), comprising: determining component validity sets for the processor component and the memory component; dividing at least one of the component validity sets into subsets (column 6, lines 55); applying component quality filters to the component designs from the component validity sets and the subsets to produce component Pareto sets of designs

(column 85 and 87, lines 5-35 and 6-21, respectively); and forming a Cartesian product of the component Pareto sets to obtain a set of system designs (column 85 and 87, lines 5-35 and 6-21, respectively).

Claim 36: A method of generating a set of partial validity (column 3, lines 57-61) predicates for a system design that includes component designs for at least a first component and a second component (column 21, lines 47-49), the method comprising: obtaining a system validity function defined by a system validity predicate (column 15, lines 28-34); and identifying coupled terms in the system validity predicate, the coupled terms including parameters (column 7, line 22) of the components; and producing a set of system designs that is a Cartesian product of component Pareto sets (column 85 and 87, lines 5-35 and 6-21, respectively).

Claim 37: The method of claim 36, wherein the system design is a processor system design and the components include a processor component and a memory component (column 16, lines 39-52).

Claim 38: The method of claim 37, further comprising expanding the coupled terms to obtain singleton terms (column 54, lines 11-21) containing parameters of only the processor component and singleton terms containing parameters of only the memory component.

Claim 39: The method of claim 36, further comprising expanding the coupled terms to obtain singleton terms (column 54, lines 11-21) containing parameters of only the first (column 21, lines 47-49) component and singleton terms containing parameters of only the second component.

Claim 40: The method of claim 39, further comprising expressing the system validity predicate in canonical form (column 53, lines 26-30-20).

Claim 41: The method of claim 36, further comprising expressing the system validity predicate in canonical form (column 53, lines 26-30-20).

Claim Rejections - 35 USC § 103

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 13 is rejected under 35 U.S.C. 103 (a) as unpatentable by Schlansker et al (U.S. Patent 6,408,428 (1999)), in view of Jacome et al. ("Lower Bound on Latency for VLIW ASIP Datapaths". IEEE (1999)).

Schlansker et al. teaches a hierarchical approach of evaluating processors (cache) and provides a method to account for each stage of changes (abstract); but doesn't teach lower bound estimates.

Jacome et al. teaches traditional lower bound estimates on latency for dataflow graphs to account for data transfer delays (abstract).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use Jacome et al. to modify Schlansker et al. since it would have been advantageous to capture the empirical results at all levels so as to modify applicable processing instructions.

Claim 13: The method of claim 12, further comprising: selecting a partial system design that includes component designs for at least one component (Schlansker: column 82, lines 23-31); obtaining a lower bound (Jacome: abstract; and pg. 262, sections 3 and 3.1) for an evaluation metric for a system design, wherein the system design includes the partial system design; and comparing an evaluation (Schlansker: column 4, lines 16-27) metric of a system that includes the partial system design to the lower bound.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is (703) 305-0365, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (703) 305-9704. The fax number for the group is 703-872-9306.

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (703) 305-3900.

October 18, 2004

THS

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER